

# 74HC283

## 4-bit binary full adder with fast carry

Rev. 03 — 11 November 2004

Product data sheet

### 1. General description

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The 74HC283 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). The 74HC283 is specified in compliance with JEDEC standard no. 7A.

The 74HC283 adds two 4-bit binary words ( $A_n$  plus  $B_n$ ) plus the incoming carry ( $C_{IN}$ ). The binary sum appears on the sum outputs ( $S_1$  to  $S_4$ ) and the out-going carry ( $C_{OUT}$ ) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \\ = S_1 + 2S_2 + 4S_3 + 8S_4 + 16C_{OUT}$$

Where (+) = plus.

Due to the symmetry of the binary add function, the 74HC283 can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic). In case of all active LOW operands the results  $S_1$  to  $S_4$  and  $C_{OUT}$  should be interpreted also as active LOW. With active HIGH inputs,  $C_{IN}$  must be held LOW when no carry in is intended. Interchanging inputs of equal weight does not affect the operation, thus  $C_{IN}$ ,  $A_1$ ,  $B_1$  can be assigned arbitrarily to pins 5, 6, 7, etc.

See the 74HC583 for the BCD version.

### 2. Features

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- High-speed 4-bit binary addition
- Cascadable in 4-bit increments
- Fast internal look-ahead carry
- Low-power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
  - ◆ HBM EIA/JESD22-A114-B exceeds 2000 V
  - ◆ MM EIA/JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+80\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ .

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### 3. Quick reference data

**Table 1: Quick reference data**

$GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $t_r = t_f = 6\text{ ns}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PHL}$ , $t_{PLH}$	propagation delay	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$				
	CIN to S1		-	16	-	ns
	CIN to S2		-	18	-	ns
	CIN to S3		-	20	-	ns
	CIN to S4		-	23	-	ns
	An or Bn to Sn		-	21	-	ns
	CIN to COUT		-	20	-	ns
	An or Bn to COUT		-	20	-	ns
$C_I$	input capacitance		-	3.5	-	pF
$C_{PD}$	power dissipation capacitance	$V_I = GND\text{ to }V_{CC}$	[1]	88	-	pF

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

### 4. Ordering information

**Table 2: Ordering information**

Type number	Package			
	Temperature range	Name	Description	Version
74HC283N	-40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HC283D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC283DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC283PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Functional diagram

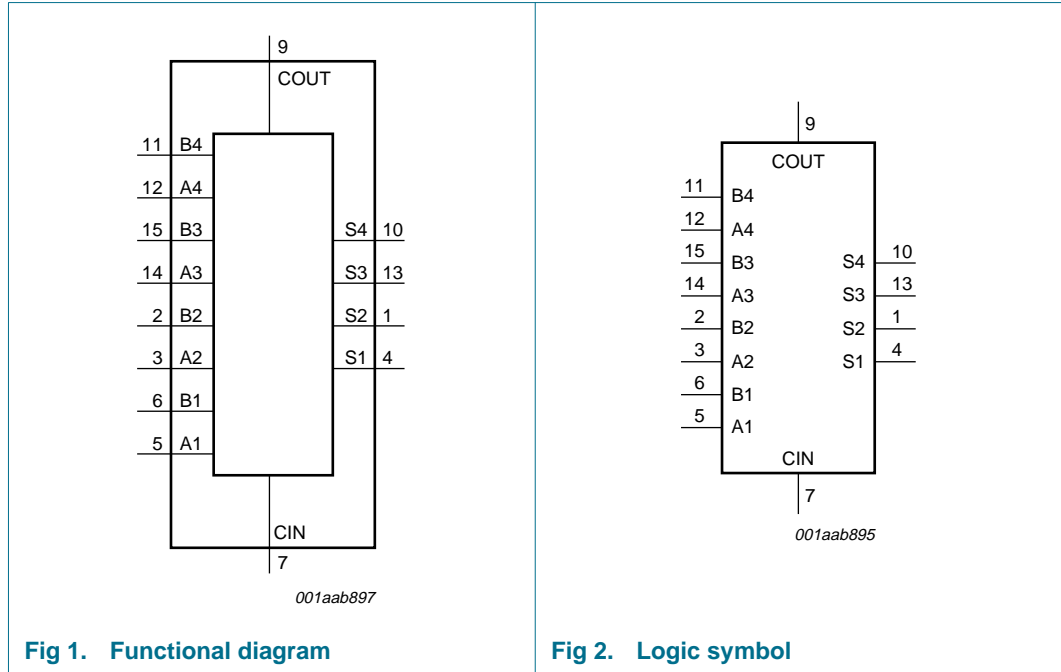


Fig 1. Functional diagram

Fig 2. Logic symbol

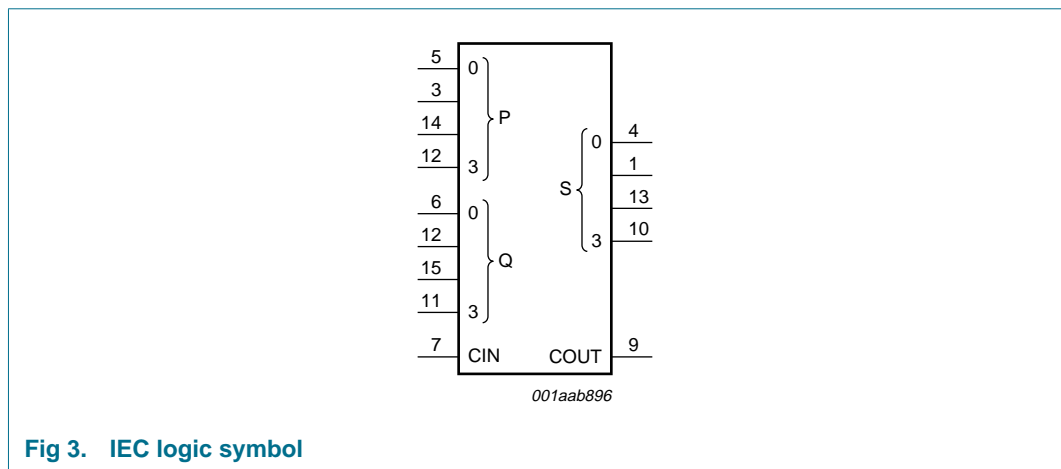


Fig 3. IEC logic symbol

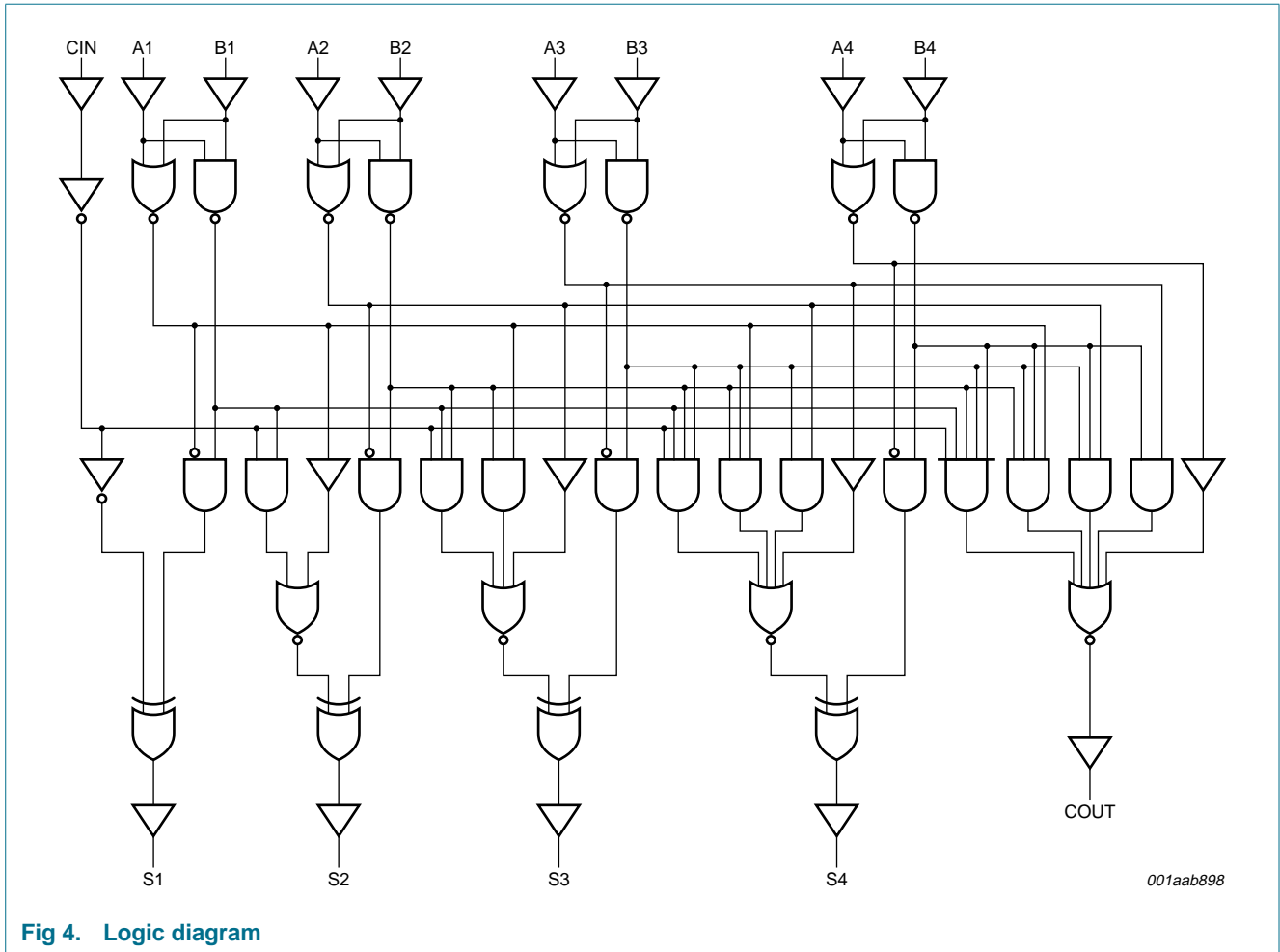


Fig 4. Logic diagram

## 6. Pinning information

### 6.1 Pinning

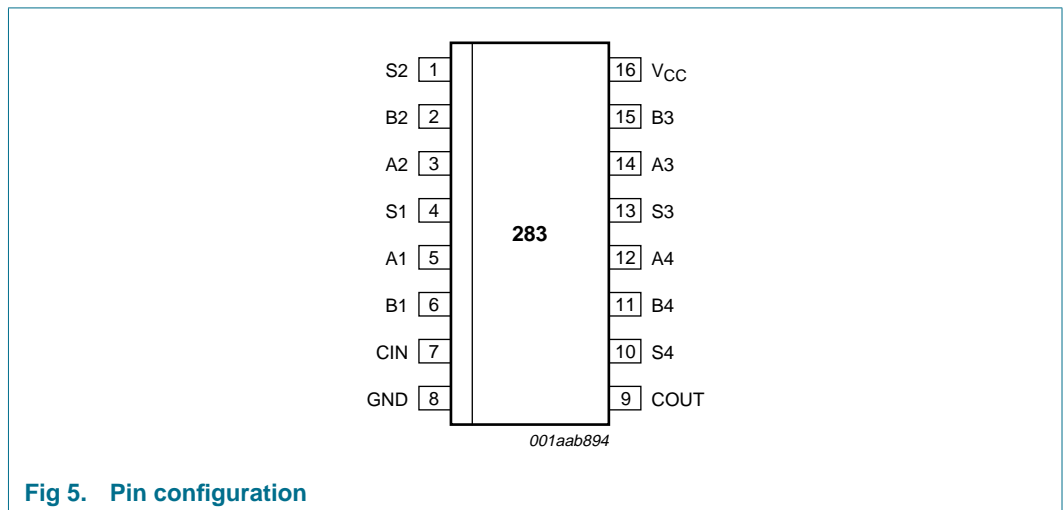


Fig 5. Pin configuration

## 6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
S2	1	sum output 2
B2	2	B operand input 2
A2	3	A operand input 2
S1	4	sum output 1
A1	5	A operand input 1
B1	6	B operand input 1
CIN	7	carry input
GND	8	ground (0 V)
COU <sup>T</sup>	9	carry output
S4	10	sum output 4
B4	11	B operand input 4
A4	12	A operand input 4
S3	13	sum output 3
B3	14	A operand input 3
A3	15	B operand input 3
V <sub>CC</sub>	16	positive supply voltage

## 7. Functional description

### 7.1 Function table

Table 4: Function table <sup>[1]</sup>

Pins	Input									Output				
	CIN	A4	A3	A2	A1	B4	B3	B2	B1	COU <sup>T</sup>	S4	S3	S2	S1
Logic levels	L	H	L	H	L	H	L	L	H	H	L	L	H	H
Active HIGH <sup>[2]</sup>	0	1	0	1	0	1	0	0	1	1	0	0	1	1
Active LOW <sup>[3]</sup>	1	0	1	0	1	0	1	1	0	0	1	1	0	0

[1] H = HIGH voltage level;  
L = LOW voltage level.

[2] Example for active HIGH:  $10 + 9 (0 + 1010 + 1001) = 19 (10011)$ .

[3] Example for active LOW:  $5 + 6 (1 + 0101 + 0110) = 12 (01100)$ .

## 8. Limiting values

**Table 5: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{OK}$	output diode current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_O$	output source or sink current	$V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$	-	$\pm 25$	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current		-	$\pm 50$	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	power dissipation				
	DIP16 package		[1] -	750	mW
	SO16, SSOP16 and TSSOP16 packages		[2] -	500	mW

[1] Above 70 °C:  $P_{tot}$  derates linearly with 12 mW/K.

[2] Above 70 °C:  $P_{tot}$  derates linearly with 8 mW/K.

## 9. Recommended operating conditions

**Table 6: Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.0	5.0	6.0	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$t_r, t_f$	input rise and fall times	$V_{CC} = 2.0\text{ V}$	-	-	1000	ns
		$V_{CC} = 4.5\text{ V}$	-	6.0	500	ns
		$V_{CC} = 6.0\text{ V}$	-	-	400	ns
$T_{amb}$	ambient temperature		-40	-	+125	°C

## 10. Static characteristics

**Table 7: Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = 25 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	V
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	V
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 2.0 V	-	0	0.1	V
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 4.5 V	-	0	0.1	V
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 6.0 V	-	0	0.1	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	µA
		V <sub>CC</sub> = 6.0 V	-	-	8.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	µA
C <sub>I</sub>	input capacitance		-	3.5	-	pF
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	V
		V <sub>CC</sub> = 4.5 V	3.15	-	-	V
		V <sub>CC</sub> = 6.0 V	4.2	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 2.0 V	1.9	-	-	V
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 4.5 V	4.4	-	-	V
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 6.0 V	5.9	-	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 4.5 V	3.84	-	-	V
		I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V	5.34	-	-	V

**Table 7: Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	-	0.1	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 4.5 V	-	-	0.33	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	-	0.33	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±1.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	80	μA
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	V
		V <sub>CC</sub> = 4.5 V	3.15	-	-	V
		V <sub>CC</sub> = 6.0 V	4.2	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		-		
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	-	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	-	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	-	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 4.5 V	3.7	-	-	V
		I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V	5.2	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		-		
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	-	0.1	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 4.5 V	-	-	0.4	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	-	0.4	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±1.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	160	μA



## 11. Dynamic characteristics

**Table 8: Dynamic characteristics**

$GND = 0\text{ V}$ ;  $t_r = t_f = 6\text{ ns}$ ;  $C_L = 50\text{ pF}$ ; see [Figure 7](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = 25\text{ °C}</math></b>						
$t_{PHL}$ , $t_{PLH}$	propagation delay CIN to S1	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0\text{ V}$	-	52	160	ns
		$V_{CC} = 4.5\text{ V}$	-	19	32	ns
		$V_{CC} = 6.0\text{ V}$	-	15	27	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	16	-	ns
	propagation delay CIN to S2	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0\text{ V}$	-	58	180	ns
		$V_{CC} = 4.5\text{ V}$	-	21	36	ns
		$V_{CC} = 6.0\text{ V}$	-	17	31	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	18	-	ns
	propagation delay CIN to S3	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0\text{ V}$	-	63	195	ns
		$V_{CC} = 4.5\text{ V}$	-	23	39	ns
		$V_{CC} = 6.0\text{ V}$	-	18	33	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	20	-	ns
	propagation delay CIN to S4	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0\text{ V}$	-	74	230	ns
		$V_{CC} = 4.5\text{ V}$	-	27	46	ns
		$V_{CC} = 6.0\text{ V}$	-	22	39	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	23	-	ns
	propagation delay An or Bn to Sn	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0\text{ V}$	-	69	210	ns
		$V_{CC} = 4.5\text{ V}$	-	25	42	ns
		$V_{CC} = 6.0\text{ V}$	-	20	36	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	21	-	ns
	propagation delay CIN to COUT	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0\text{ V}$	-	63	195	ns
		$V_{CC} = 4.5\text{ V}$	-	23	39	ns
		$V_{CC} = 6.0\text{ V}$	-	18	33	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	20	-	ns
	propagation delay An or Bn to COUT	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0\text{ V}$	-	63	195	ns
		$V_{CC} = 4.5\text{ V}$	-	23	39	ns
		$V_{CC} = 6.0\text{ V}$	-	18	33	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	20	-	ns

**Table 8: Dynamic characteristics ...continued**  
*GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF; see [Figure 7](#).*

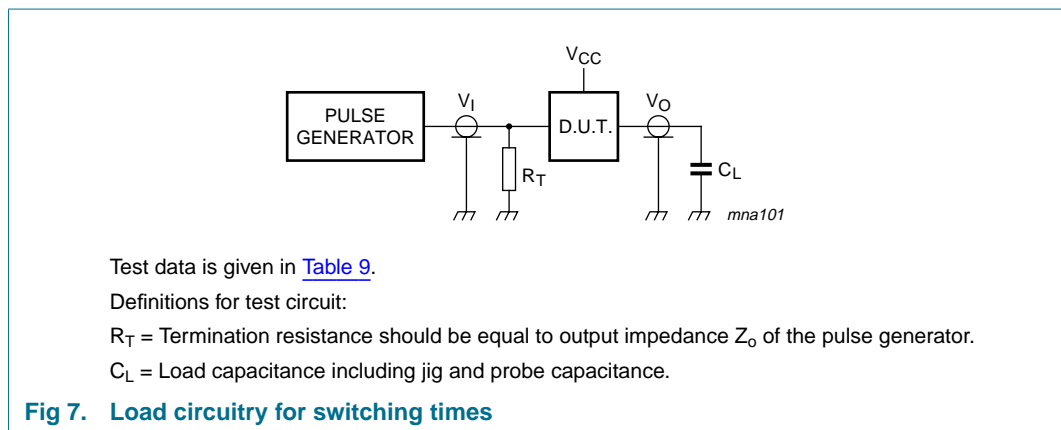
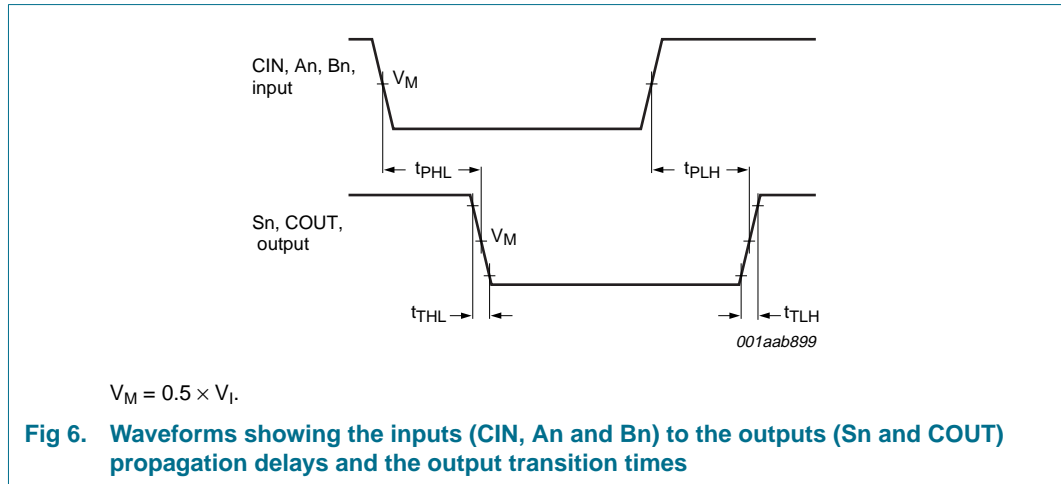
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{THL}, t_{TLH}$	output transition time	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0$ V	-	19	75	ns
		$V_{CC} = 4.5$ V	-	7	15	ns
		$V_{CC} = 6.0$ V	-	6	13	ns
$C_{PD}$	power dissipation capacitance	$V_I = GND$ to $V_{CC}$	[1] -	88	-	pF
<b><math>T_{amb} = -40</math> °C to <math>+85</math> °C</b>						
$t_{PHL}, t_{PLH}$	propagation delay CIN to S1	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0$ V	-	-	200	ns
		$V_{CC} = 4.5$ V	-	-	40	ns
	propagation delay CIN to S2	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0$ V	-	-	225	ns
		$V_{CC} = 4.5$ V	-	-	45	ns
	propagation delay CIN to S3	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0$ V	-	-	245	ns
		$V_{CC} = 4.5$ V	-	-	49	ns
	propagation delay CIN to S4	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0$ V	-	-	290	ns
		$V_{CC} = 4.5$ V	-	-	58	ns
	propagation delay An or Bn to Sn	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0$ V	-	-	265	ns
		$V_{CC} = 4.5$ V	-	-	53	ns
	propagation delay CIN to COUT	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0$ V	-	-	245	ns
		$V_{CC} = 4.5$ V	-	-	49	ns
	propagation delay An or Bn to COUT	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0$ V	-	-	245	ns
		$V_{CC} = 4.5$ V	-	-	49	ns
$t_{THL}, t_{TLH}$	output transition time	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0$ V	-	-	95	ns
		$V_{CC} = 4.5$ V	-	-	19	ns
		$V_{CC} = 6.0$ V	-	-	16	ns

**Table 8: Dynamic characteristics ...continued**  
*GND = 0 V;  $t_r = t_f = 6 \text{ ns}$ ;  $C_L = 50 \text{ pF}$ ; see [Figure 7](#).*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{\text{amb}} = -40 \text{ }^\circ\text{C to } +125 \text{ }^\circ\text{C}</math></b>						
$t_{\text{PHL}}, t_{\text{PLH}}$	propagation delay CIN to S1	see <a href="#">Figure 6</a>				
		$V_{\text{CC}} = 2.0 \text{ V}$	-	-	240	ns
		$V_{\text{CC}} = 4.5 \text{ V}$	-	-	48	ns
		$V_{\text{CC}} = 6.0 \text{ V}$	-	-	41	ns
	propagation delay CIN to S2	see <a href="#">Figure 6</a>				
		$V_{\text{CC}} = 2.0 \text{ V}$	-	-	270	ns
		$V_{\text{CC}} = 4.5 \text{ V}$	-	-	54	ns
		$V_{\text{CC}} = 6.0 \text{ V}$	-	-	46	ns
	propagation delay CIN to S3	see <a href="#">Figure 6</a>				
		$V_{\text{CC}} = 2.0 \text{ V}$	-	-	295	ns
		$V_{\text{CC}} = 4.5 \text{ V}$	-	-	59	ns
		$V_{\text{CC}} = 6.0 \text{ V}$	-	-	50	ns
	propagation delay CIN to S4	see <a href="#">Figure 6</a>				
		$V_{\text{CC}} = 2.0 \text{ V}$	-	-	345	ns
		$V_{\text{CC}} = 4.5 \text{ V}$	-	-	69	ns
		$V_{\text{CC}} = 6.0 \text{ V}$	-	-	59	ns
	propagation delay An or Bn to Sn	see <a href="#">Figure 6</a>				
		$V_{\text{CC}} = 2.0 \text{ V}$	-	-	315	ns
		$V_{\text{CC}} = 4.5 \text{ V}$	-	-	63	ns
		$V_{\text{CC}} = 6.0 \text{ V}$	-	-	54	ns
	propagation delay CIN to COUT	see <a href="#">Figure 6</a>				
		$V_{\text{CC}} = 2.0 \text{ V}$	-	-	295	ns
		$V_{\text{CC}} = 4.5 \text{ V}$	-	-	59	ns
		$V_{\text{CC}} = 6.0 \text{ V}$	-	-	50	ns
	propagation delay An or Bn to COUT	see <a href="#">Figure 6</a>				
		$V_{\text{CC}} = 2.0 \text{ V}$	-	-	295	ns
		$V_{\text{CC}} = 4.5 \text{ V}$	-	-	59	ns
	$V_{\text{CC}} = 6.0 \text{ V}$	-	-	50	ns	
$t_{\text{THL}}, t_{\text{TLH}}$	output transition time	see <a href="#">Figure 6</a>				
		$V_{\text{CC}} = 2.0 \text{ V}$	-	-	110	ns
		$V_{\text{CC}} = 4.5 \text{ V}$	-	-	22	ns
	$V_{\text{CC}} = 6.0 \text{ V}$	-	-	19	ns	

[1]  $C_{\text{PD}}$  is used to determine the dynamic power dissipation ( $P_{\text{D}}$  in  $\mu\text{W}$ ).  
 $P_{\text{D}} = C_{\text{PD}} \times V_{\text{CC}}^2 \times f_i \times N + \sum(C_L \times V_{\text{CC}}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $C_L$  = output load capacitance in pF;  
 $V_{\text{CC}}$  = supply voltage in V;  
 $N$  = number of inputs switching;  
 $\sum(C_L \times V_{\text{CC}}^2 \times f_o)$  sum of outputs.

## 12. Waveforms



**Table 9: Test data**

Supply	Input		Load
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$
2.0 V	$V_{CC}$	6 ns	50 pF
4.5 V	$V_{CC}$	6 ns	50 pF
6.0 V	$V_{CC}$	6 ns	50 pF
5.0 V	$V_{CC}$	6 ns	15 pF

## 13. Application information

[Figure 8](#) shows a 3-bit adder using the 74HC283. Trying the operand inputs of the fourth adder (A4 and B4) LOW makes S4 dependent on, and equal to, the carry from the third adder.

[Figure 9](#), based on the same principle, shows a method of dividing the 74HC283 into a 2-bit and 1-bit adder. The third stage adder (A3, B3 and S3) is used simply as means of transferring the carry into the fourth stage (via A3 and B3) and transferring the carry from

the second stage on S3. As long as A3 and B3 are the same, HIGH or LOW, they do not influence S3. Similarly, when A3 and B3 are the same, the carry into the third stage does not influence the carry out of the third stage.

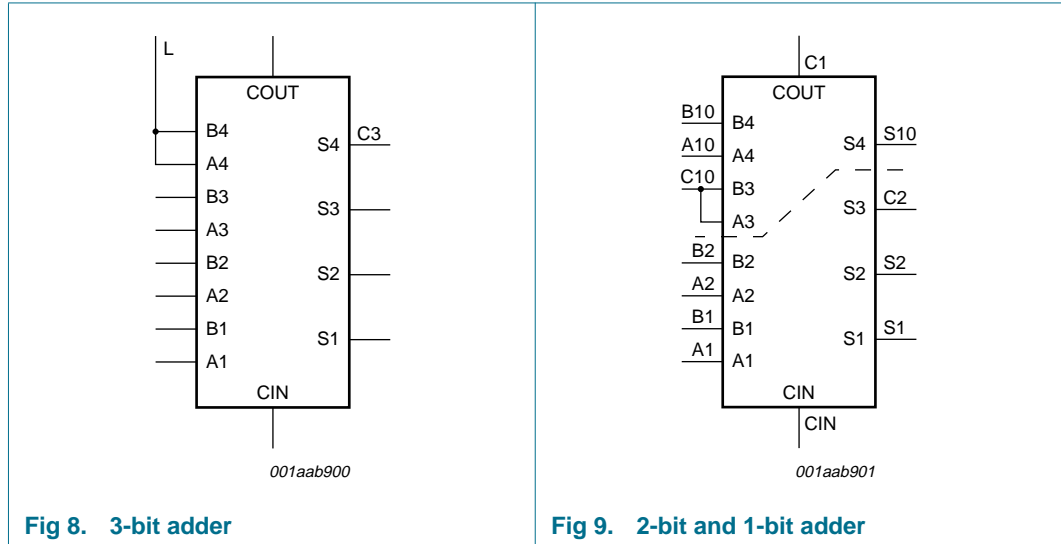


Fig 8. 3-bit adder

Fig 9. 2-bit and 1-bit adder

Figure 10 shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S1, S2 and S3 produce a binary number equal to the number inputs (I1 to I5) that are HIGH.

Figure 11 shows a method of implementing a 5-input majority gate. When three or more inputs (I1 to I5) are HIGH, the output M5 is HIGH.

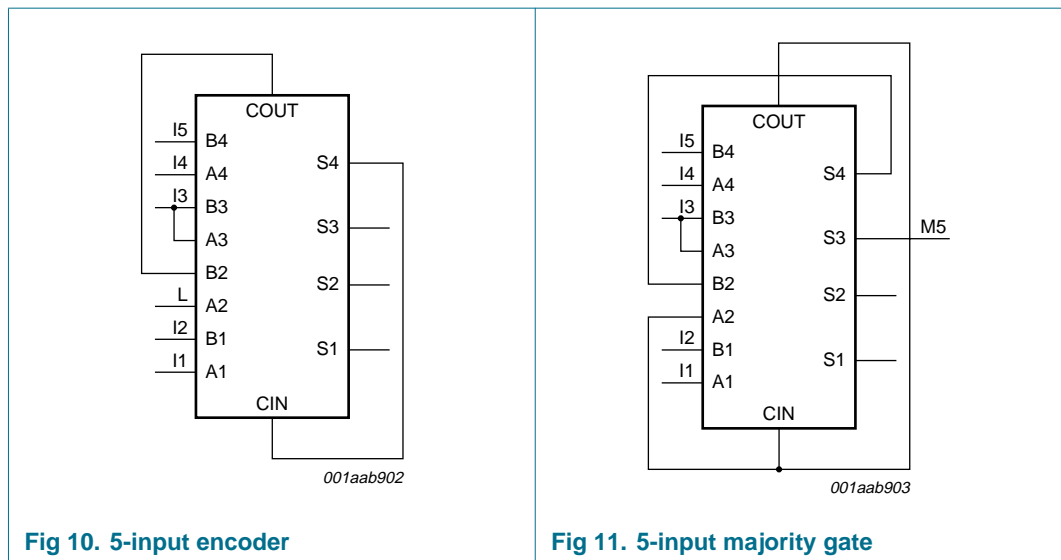


Fig 10. 5-input encoder

Fig 11. 5-input majority gate

14. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

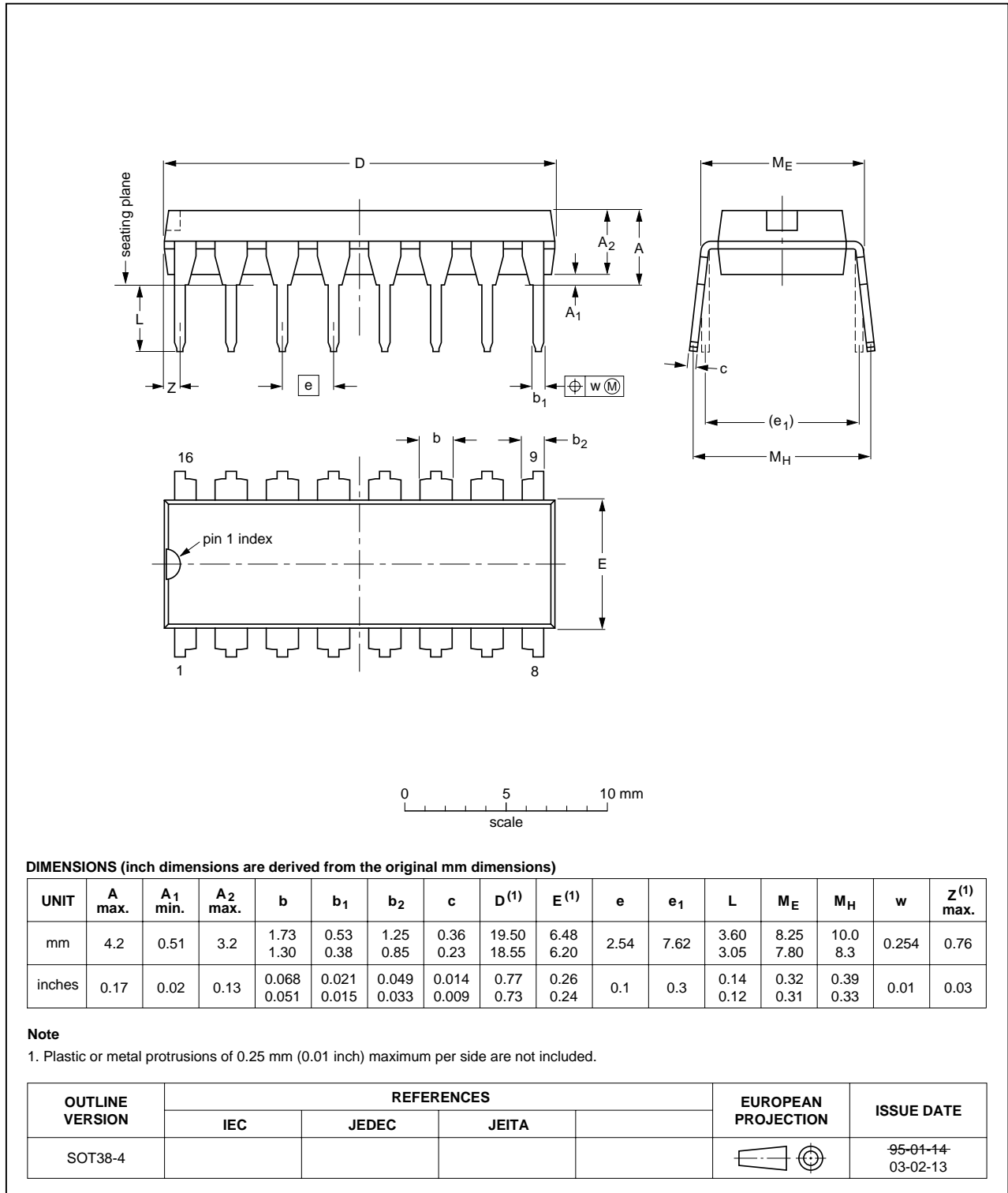


Fig 12. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

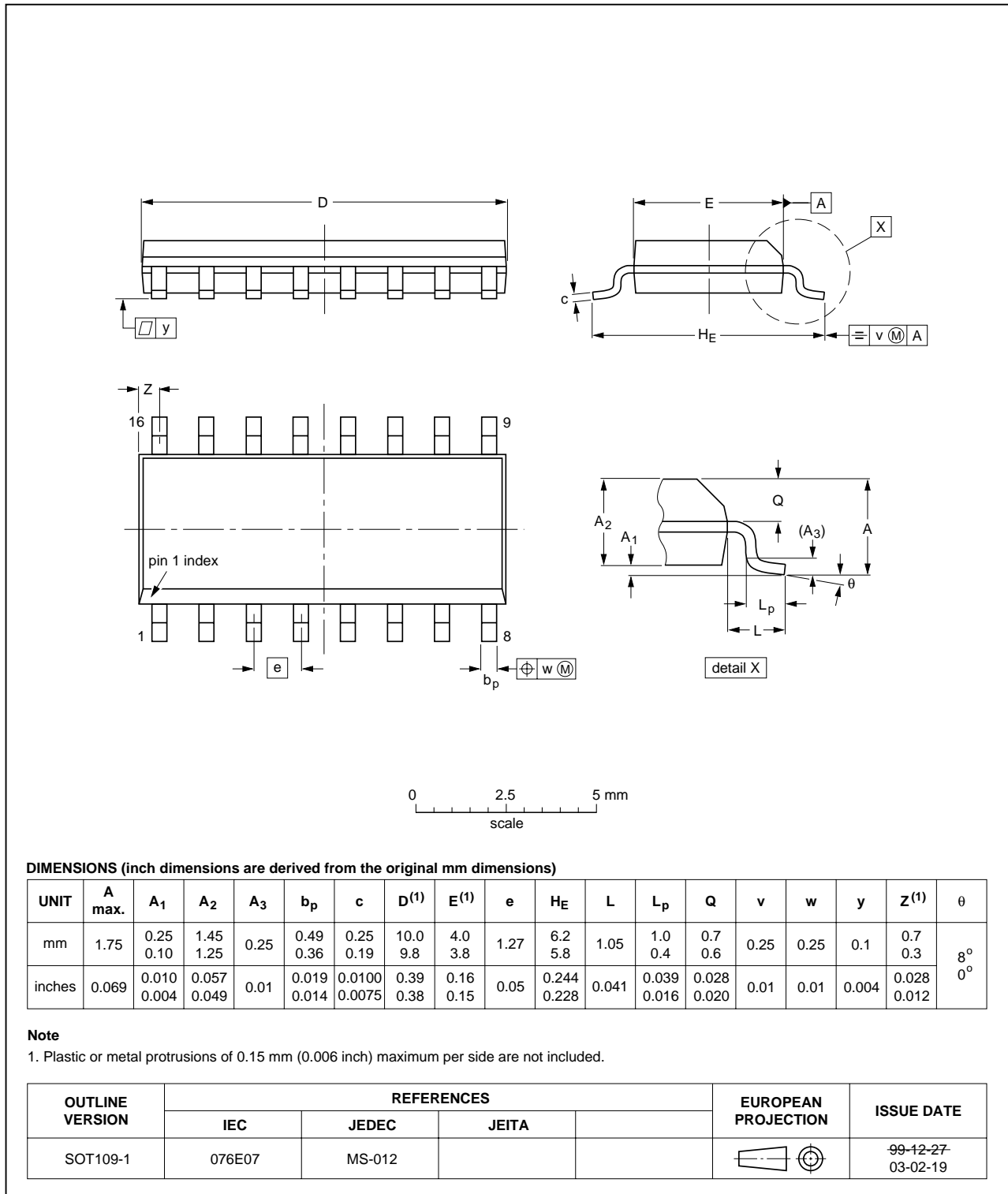


Fig 13. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

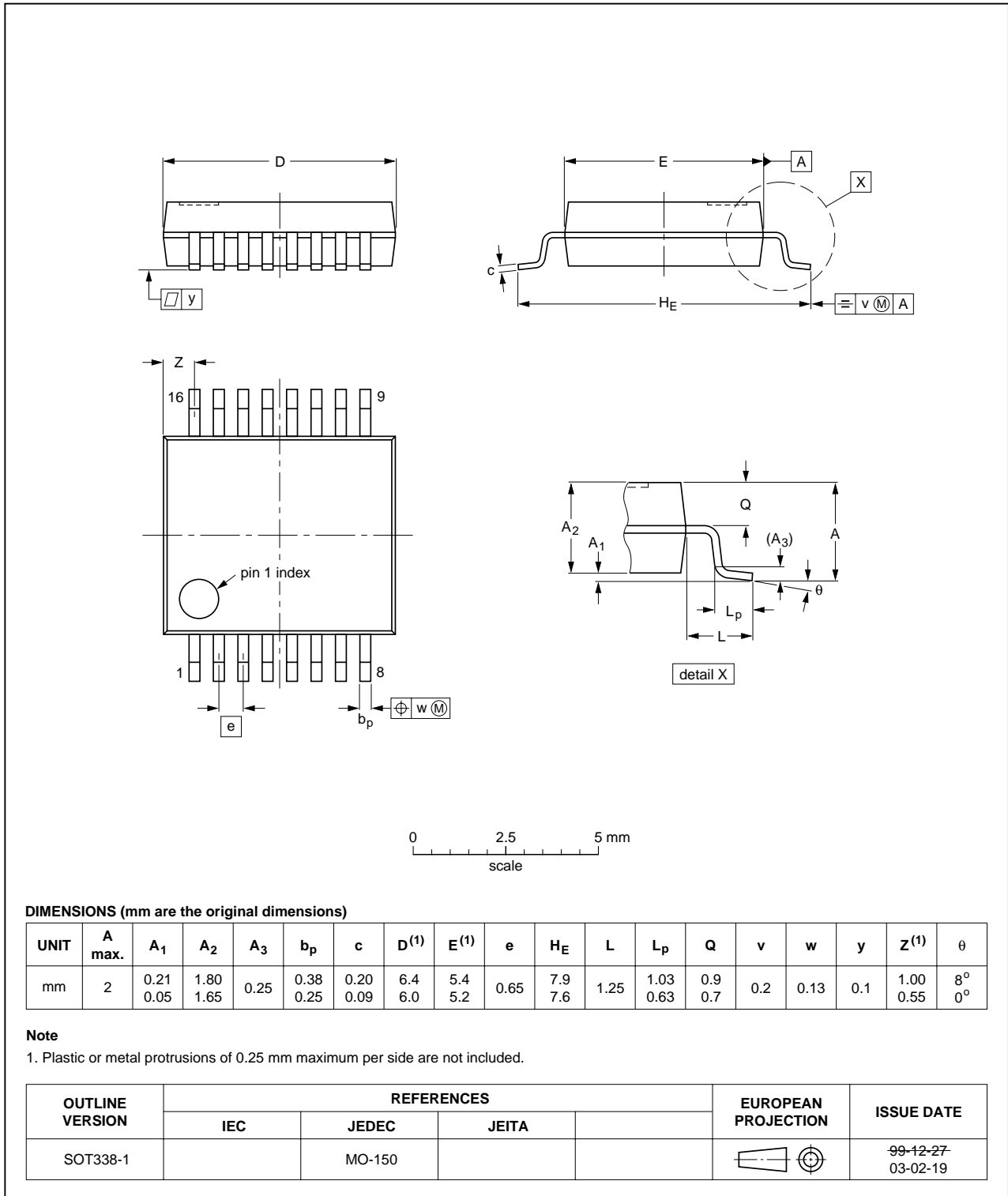


Fig 14. Package outline SOT338-1 (SSOP16)



TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



Fig 15. Package outline SOT403-1 (TSSOP16)

## 15. Revision history

**Table 10: Revision history**

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74HC283_3	20041111	Product data sheet	-	9397 750 13811	74HC_HCT283_CNV_2
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors.</li><li>• Removed type number 74HCT283.</li><li>• Inserted family specification.</li></ul>				
74HC_HCT283_CNV_2	19970828	Product specification	-	-	74HC_HCT283_1
74HC_HCT283_1	19901201	Product specification	-	-	-

## 16. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> <sup>[3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 17. Definitions

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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## 19. Contact information

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